REMARKS

Claims 1-3, 7-10, 12, 14, 16-19, 21, 23, 25, 26, and 29 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Cousin (U.S. Patent No. 6.725,357).

This rejection is respectfully traversed for the following reasons.

Claim 1 recites a computer processor comprising:

(a) a decode unit for decoding a stream of instruction packets from a memory, each instruction packet comprising a plurality of instructions;

(b) a first processing channel comprising a plurality of functional units and operable to perform control processing operations;

(c) a second processing channel comprising a plurality of functional units and operable to perform data processing operations;

wherein the decode unit is operable to receive an instruction packet and to detect if the instruction packet defines (i) a plurality of control instructions or (ii) a plurality of instructions one or more of which is a data processing instruction, and wherein when the decode unit detects that the instruction packet comprises a plurality of control instructions said control instructions are supplied to the first processing channel for execution in program order.

Independent claim 26 recites a method of operating a computer processor which comprises first and second processing channels, each having a plurality of functional units, wherein the first processing channel is capable of performing control processing operations and the second processing channel is capable of performing data processing operations, the method comprising:

(a) receiving a sequence of instruction packets from a memory, each of said instruction packets comprising a plurality of instructions defining operations;

(b) decoding each instruction packet in turn by determining if the instruction packet defines:

(i) a plurality of control instructions; or

(ii) at least one data processing instruction, and

wherein when the decode unit detects that the instruction packet comprises a plurality of control instructions supplying said plurality of control instructions to said first processing channel for execution in sequence.

Independent claim 29 recites a computer readable medium bearing an instruction set for a computer including a first class of instruction packets each comprising a plurality of control instructions for execution sequentially and a second class of instruction packets each comprising at least a data processing instruction and a further instruction for execution contemporaneously, said further instruction being selected from one or more of: a memory access instruction; a control instruction; and a data processing instruction.

Hence, among other features, each of the independent claims requires the instruction packet to comprise a plurality of control instructions.

It is well settled that anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989).

The Examiner takes the position that col. 4, lines 15-19, and col. 7, lines 3-15 disclose that the instruction packet comprises a plurality of control instructions.

Considering the reference, col. 4, lines 15-19, discloses that the micro-instruction generator 10 dispatches micro-instructions to the queues in a format which depends on the intended execution unit.

Col. 7, lines 3-15, discloses that the instruction in the flip-flop 336 is output to one of the multiplexers 314 or 318.

Hence, the reference does not expressly disclose that the instruction packet comprises a plurality of control instructions.

It appears that the Examiner relied upon inherency without expressly indicating such reliance. In particular, the Examiner speculates that "it is clear from all of the cites" that Cousin distinguishes between control instructions (address and branch) and data instructions, as illustrated by two separate datapaths shown in FIG. 3.

It is noted that the diagram in FIG. 3 does not indicate that the instruction packet comprises a plurality of control instructions.

The Examiner is respectfully reminded that inherency requires certainty, not speculation. ***In re Rijckaert***, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***In re King***, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); ***W. L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); ***In re Oelrich***, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); ***In re Wilding***, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

The Examiner provided no factual basis upon which to conclude that Cousin's micro-instructions **necessarily** contain multiple control instructions. As one skilled in the art would realize, dispatching micro-instructions to queues does not require a micro-instruction to contain multiple control instructions.

Moreover, a statement of the inventor of the present application is provided herewith as evidence that one skilled in the art would realize that multiple control instructions are not necessarily present in each of Cousin's instructions.

Consideration of this statement is respectfully requested.

Hence, Cousin neither expressly nor inherently discloses that an instruction packet comprises a plurality of control instructions, as independent claims 1, 16 and 29 recite.

Accordingly, Cousin does not describe the claimed invention within the meaning of 35 U.S.C. § 102, ***Kalman v. Kimberly-Clark Corp., Richardson v. Suzuki Motor Co., supra.*** Applicant, therefore, respectfully submits that the rejection of claims 1-3, 7-10, 12, 14, 16-19, 21, 23, 25, 26, and 29 under 35 U.S.C. § 102 as anticipated by Cousin is untenable and should be withdrawn.

Claims 4-5 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin in view of Takayama. Claims 6, 22, and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin. Claims 13 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin in view of DeHon. Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin in view of Simonen et al. Claims 27 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin in view of Tanenbaum.

The rejected claims depend from claim 1 or 26. Therefore, they are defined over the prior art at least for the reasons presented above in connection with the respective independent claims.

In view of the foregoing, and in summary, claims 1-29 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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